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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,874	11/26/2003	Takashi Kobayashi	XA-10000	6095
181	7590	01/12/2006	EXAMINER	
MILES & STOCKBRIDGE PC 1751 PINNACLE DRIVE SUITE 500 MCLEAN, VA 22102-3833			ERDEM, FAZLI	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/721,874	Applicant(s) KOBAYASHI ET AL.	
	Examiner Fazli Erdem	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-21 and 23-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4,9-11,13,18,20,21,23,28 and 29 is/are rejected.
- 7) ☒ Claim(s) 5-8,12,14-17,19 and 24-27 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election restriction that was issued by examiner on August 26, 2004 has been vacated.

Allowable Subject Matter

1. Claims 5-8, 12, 14-17, 19 and 24-27 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 4, 9-11, 13, 18, 20, 21, 23, 28 and 29 rejected under 35 U.S.C. 103(a) as being unpatentable over Eitan (6,011,725) in view of Fan et al. (6,834,013) further in view of Taira et al. (6,410,412)

Regarding Claims 1, 2, 4, 9-11, 13, 18, 20, 21, 23, 28 and 29, Eitan discloses a two bit non-volatile electrically erasable and programmable semiconductor memory cell utilizing asymmetrical charge trapping where in Figs. 1-5, it is disclose a first insulator film 56 formed above a semiconductor substrate 62, silicon nitride dots charge trapping layer 54 formed on the first insulator layer 56, a second insulator film formed on silicon nitride dots charge trapping layer, a conductive film 50 formed above the second insulator film 52, a channel region formed in semiconductor substrate 62 and disposed between semiconductor source/drain regions 58 and 60. Eitan fails to disclose the

required programming structure and the required heights of the insulating and the dot/particulate layers. However, Fan et al. disclose a method for programming and erasing non-volatile memory with nitride tunneling layer where in abstract section and in columns 1 and 3, programming is performed by injecting charges from channel region into silicon nitride charge trapping layer. Furthermore, Taira et al. disclose methods for fabricating memory devices where in Fig. 13, the insulating layers 6 and 11 have heights greater than the height of the dot/particulate layer 9.

Regarding Claim 2, Figs. 1-5 of Eitan disclose the required programming direction.

Regarding Claim 9, silicon nitride dots charge trapping layer 54 of Eitan is present as a single layer.

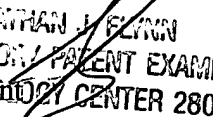
It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required programming by injection of charges from channel region into silicon nitride charge trapping region and the required height of the insulating and the particle/dot layers, in order to have a nonvolatile semiconductor memory cell with increased performance and reliability.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.


NATHAN J. FLYNN
SOFT PATENT EXAMINER
EBC CENTER 2800

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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January 6, 2006